In the Claims:

Please cancel claim 1 without prejudice.

Please amend claims 2-15 as follows:

2. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of mounting silicon capacitors directly onto the carrier package.

3. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of mounting silicon resistors directly onto the carrier package.

4. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of using flip-chip mounting methods for assembling silicon chips onto the carrier package.

5. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of generating a respective physical design for customized passive devices, a logic chip, and a chip carrier includes the steps of generating a physical design for a silicon capacitor chip having a selected capacitor shape.

6. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of generating a respective physical design for customized passive devices, a logic chip, and a chip carrier includes the steps of generating a physical design for a silicon capacitor chip having a selected capacitor size.

7. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of generating a respective physical design for customized passive devices, a logic chip, and a chip carrier includes the steps of generating a physical design for a silicon capacitor chip having a selected number of capacitor connections.

8. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of receiving system design inputs for a package arrangement includes the steps of receiving voltage and current limits.

9. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of receiving system design inputs for a package arrangement includes the steps of receiving system targets and a frequency specification.

10. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of receiving system design inputs for a package arrangement includes the steps of receiving logic chip parameters.

11. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of receiving system design inputs for a package arrangement includes the steps of receiving chip carrier package specifications.

12. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of receiving system design inputs for a package arrangement includes the steps of receiving cost target specifications.

13. (currently amended) A method as recited in ~~claim 1~~ claim 14 wherein the step of fabricating silicon devices utilizing the generated respective physical design for customized passive devices and the logic chip includes the steps of defining silicon chip

decoupling capacitors and silicon resistors from selected areas of a silicon wafer used for forming the logic chip.

14. (currently amended) A method ~~as recited in claim 1 wherein the step of fabricating silicon devices includes~~ for implementing customized silicon wafer chip carrier passive devices comprising the steps of:

receiving system design inputs for a package arrangement;

generating a respective physical design for customized passive devices, a logic chip, and a chip carrier;

fabricating silicon devices utilizing the generated respective physical design for customized passive devices and the logic chip including the steps of dicing silicon chip decoupling capacitors from a peripheral area of a silicon wafer;

fabricating a carrier package; and

assembling the fabricated silicon devices on the carrier package.

15. (currently amended) Apparatus for implementing customized silicon wafer chip carrier passive devices on a carrier package arrangement comprising:

a silicon passive devices customizing program for receiving system design inputs for a carrier package arrangement;

said silicon passive devices customizing program for generating a respective physical design for customized passive devices, a logic chip, and a chip carrier; for fabricating silicon devices utilizing the generated respective physical design for customized passive devices and the logic chip including dicing silicon chip decoupling capacitors from a peripheral area of a silicon wafer and for fabricating a carrier

package; and

said silicon passive devices customizing program for assembling the fabricated silicon devices onto the carrier package.

16. (original) Apparatus for implementing customized silicon wafer chip carrier passive devices as recited in claim 15 wherein the system design inputs include at least one of voltage and current limits; system targets and a frequency specification; logic chip parameters; chip carrier package specifications; and cost target specifications.

17. (original) Apparatus for implementing customized silicon wafer chip carrier passive devices as recited in claim 15 wherein said silicon passive devices customizing program for assembling the fabricated silicon devices onto the carrier package includes said silicon passive devices customizing program for assembling the fabricated silicon capacitors directly onto the carrier package.

18. (original) Apparatus for implementing customized silicon wafer chip carrier passive devices as recited in claim 15 wherein said silicon passive devices customizing program for generating a respective physical design for customized passive devices includes said silicon passive devices customizing program for generating a physical design for a silicon capacitor chip having a selected capacitor shape; a selected capacitor size; and a selected number of capacitor connectors.